IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Adkisson et al.
Serial No. 09/691,353 Group Art Unit 2823
Filed October 18, 2000 Examiner K. Nguyen
For METHOD OF FABRICATING SEMICONDUCTOR SIDE WALL FIN

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. §1.132
OF
JAMES W. ADKISSON

Sir:

JAMES W. ADKISSON declares as follows:

1. I received a B.S. in Physics from MIT, with a Masters and PhD from Stanford University, where I worked on hetero-epitaxial growth of GaAs on Si for optoelectronic applications.

2. I am employed by International Business Machines Corporation at their Microelectronics facility in Burlington, Vermont, where I am a Senior Technical Staff Member. I have worked at IBM for fourteen years in semiconductor technology.

3. I have reviewed the subject patent application, including the claims, and the examiner's remarks as contained in the Office Action mailed on February 23, 2006. I have also reviewed the U.S. Patent No. 6,479,847 to Misewich et al.

4. The epitaxial layers in Misewich are all grown vertically from the substrate and do not disclose "a semiconductor region ... upon one of whose opposite vertical sides said first channel was grown". See col 8, lines 8-11, col 8, lines 22-28, and figs. 6, 8 and 10 where it is clear that the channel region and the electrically active part of the FET are not at the transition region where any vertical side might have an epitaxial growth. Note that Misewich never discusses the transition region between the n and p regions shown in Figure 8, nor do any of his electrodes allow an active device in this region. For example, no gate electrode 1002 sits in the transition region between 602 and 801.

5. In Misewich, gates (603, 802) and gate electrodes (1002) are never formed adjacent to the sidewalls and do not disclose "forming a gate that contacts a top surface and two side surfaces of the first and second epitaxially grown channels...". In Misewich, they are epitaxially grown vertically from the substrate on top of the channel. Again, see col 8, lines 8-11; col 8, lines 22-28 and Figs. 6, 8, and 10.

6. The present invention claims an epitaxially grown layer (204 in Figs. 2A, 2B and 2C). It is claimed that this layer is grown from a vertical surface (110 in Fig. 2B, "on whose opposite vertical sides said first channel was grown"). As indicated in paragraphs 4 and 5, above, the epitaxial layers in Misewich are grown vertically from the substrate, that is, from a horizontal surface.

7. With regard to claim 15, nowhere does Misewich teach "an etch stop layer on an exposed side surface of each of the first and second semiconductor lines". Nowhere does Misewich teach "epitaxially growing first and second semiconductor layers on each etch stop layer". Nowhere does Misewich teach "filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source and drain with an oxide fill."

8. Nowhere does Misewich teach "etching a portion of the oxide fill to form an area that defines a gate..." In Figure 1 of Misewich, the conductive gate layers are 104 which are placed horizontally without an etch. The gate via

2010 is only a contact to the gate, not the gate itself. In Figure 10 neither the gate layers 603 and 802, nor the gate electrode 1002, are formed by etching an oxide fill (and there is no "oxide fill" disclosed in Misewich).

9. As to the additional element in claim 16, Misewich does not disclose any oxide fill, as discussed above, so he certainly does not discuss etching the fill to expose the layers.

10. As to the additional element in claim 17, the Examiner's reference to 602 as being an "...epitaxially grown silicon layer(s)" is not supported anywhere in Misewich, which refers to 602 as a "P-type Mott-transition layer 602 (e.g., La_2CuO_4)" (col 8, line 8-9), which silicon is most certainly not, or more generally an "epitaxially grown cuprate material" (col 1, lines 40-42), which again, silicon is not.

11. As to the additional element in claim 18, Misewich never discusses silicon dioxide. The Examiner references col 8, lines 16-21, as referring to silicon dioxide. However, this passage does not discuss silicon dioxide. Instead, it discusses only a "gate oxide" layer 603, which in the previous paragraph (col 8 lines 9-10) is discussed as strontium titanate.

12. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above referenced application and any patent issuing thereon.

Date: May 22, 2006

JAMES W. ADKISSON